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FPGA Based Face Detection System using Xilinx System Generator

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Abstract: In the field of face recognition and establishment of face database, face detection is a crucial step. Image Features are the basis for most of the real time image processing applications. Skin color is one of the prime features of image. A variety of skin color tones along with other constraints on image capturing within a given background make face detection a challenging task of image processing for surveillance and security applications. Processing color information is faster than processing other facial features. In this paper skin color detection YCbCr model is implemented on FPGA using Xilinx System Generator based on Hardware/Software Co-simulation. Xilinx System Generator is a DSP design tool from Xilinx that enables the use of the Math Works model-based Simulink design environment for FPGA design.

Keywords: Image Processing, FPGA, Xilinx System Generator.

I. INTRODUCTION

Face detection is currently an interesting research topic because it is used in various applications. Human face detection is concerned with finding the location and size of every human face in a given image. Face detection plays a very important role in human computer interaction field. It represents the first step in a fully automatic face recognition, facial features detection, and expression recognition. In the recent decade, the security systems based on the information about a user's identity, like fingerprint and sound print, but now it depends on facial features. The extraction of these features from images is done by using face recognition techniques, and that computers of the security systems can then react accordingly. The most crucial process is to detect faces and owing to its numerous applications, a face detection system must be accurate. Researchers in the field of image and video processing have made it possible to detect multiple faces in an image. There are various face detection challenges that affect the detection rate such as different face sizes, various face orientation, changeable lighting condition, presence of non skin component on face etc [1].

Many researchers have been investigated in the field of face detection but most of the research is done on the PC or software platform. FPGA based face detection researches are less due to hardware difficulties. The face detection is classified into following methods:

- Knowledge-Based
- Feature invariant based
- Template matching
- Appearance based

The purpose of this paper is to develop face detection system based on feature invariant method using Xilinx system generator with the help of hardware software co-simulation approach.

II. RELATED WORKS

Literature survey say that The Field-programmable gate array (FPGA) system is capable of high speed parallel processing and build a hierarchy design, which is powerful and fast enough to fulfill all the need of functionality, making it preferable over general purpose processor or micro-controller and has the added advantage of being reconfigurable for future development. Also Benefits of FPGA Technology like high performance, low Time to Market, low cost, high reliability, and Long-Term Maintenance. Real time applications FPGAs are perfectly suitable for applications in time-critical systems. The System Generator environment allows for the Xilinx line of FPGAs to be interface directly with Matlab Simulink. In addition there are several cost effective development boards available on the market that can be utilized for the software design development phase.

A. Xilinx System Generator (XSG)

System Generator is part of the Xilinx ISE Design Suite and provides Xilinx DSP Blockset such as adders, multipliers, registers, filters and memories for application specific design. These blocks use the Xilinx IP core generators to deliver optimized results for the selected device.When we use System Generator Xilinx FPGAs or RTL design methodologies is not required. Designs are captured in the DSP friendly Simulink modelling environment using a Xilinx specific Blockset. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. Advantage of using Xilinx system generator for hardware implementation is that Xilinx Blockset provides close integration with MATLAB Simulink that helps in co-simulating the FPGA module with pixel vector provided by MATLAB Simulink Blocks[4].

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B. Skin Color Model

Skin color is one of the most important features in the human face. Detection of skin color in color images is a very popular and useful technique for face detection. Many techniques have reported for locating skin color regions in the input image. The RGB format is not used because RGB components are subject to the lighting conditions which causes the face detection may fail when the lighting conditions change. Feature-based face detection techniques may use skin color information to detect faces in color images having complex background. The skin detector detects whether certain regions in a color image represent human skin or not. It must define certain decision rules to discriminate between skin and non-skin pixels. To build these rules, a human skin model must be built. Several skin color-modeling methods have been introduced [3].

C. Skin Color Detection using YCbCr

In the YCbCr color model, the luminance information is contained in Y component and the chrominance information is in Cb and Cr. Many research studies found that the chrominance components of the skin-tone color are independent of the luminance component. Hence the Cb, Cr components are used to model the distribution of skin colors. It is well known that different people have different skin color appearance, but these differences lie mostly in the color intensity not in the color itself. Cb-Cr color space was chosen in our work for many reasons first is, it contains no information about luminance which yields a more general skin color model and also it has only two components which helps to speed up the calculations. The transformation between RGB and YCbCr model is represented by the following equations:

$$Y = 16 + 65.738R + 129.057G + 25.064B \quad (1)$$
$$Cb = 128 - 37.945R - 74.494G + 112.439B \quad (2)$$
$$Cr = 128 + 112.439R - 94.154G - 18.285B \quad (3)$$

The range in which Y, Cb and Cr components are scaled is given as, Y=16 to 235, where 16 for black and 235 for white. Cb=16 to 240 and Cr =16 to 240. As the luminous and chrominance components can be treated separately, the influence of illumination can be removed during processing of an image.

a.

III. PROPOSED APPROACH

A. System Flow

Methodology includes designing of face detection system in MATLAB using Xilinx System Generator (simulink block). Model generates HDL code and netlist that can be Synthesized and optimized using ISE 13.2. It is implemented over Virtex-5 FPGA. Flow of Xilinx system generator is depicted in figure 1. It finally generates bit stream file that can be loaded into FPGA. Significant drawback of traditional approach used for hardware implementation is that it uses a high level language for coding; finally generating bit stream file. Xilinx introduced the advanced system modeling tool (Xilinx System Generator) that has easy to understand system development approach [5].

b.

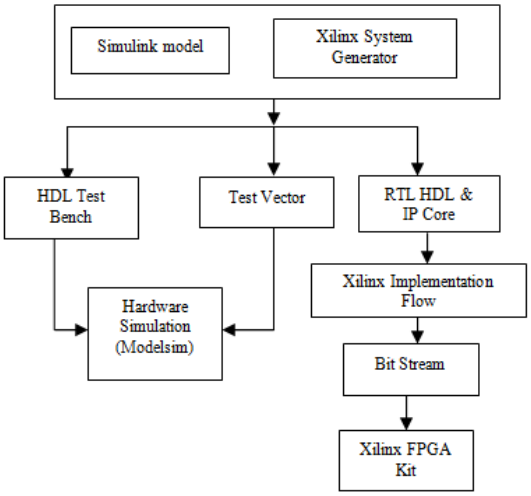

Figure 1: Block diagram for system generator design flow

Flow of the face detection unit is depicted in Figure 2. It includes image pre-processing and post-processing operations. They make data available in suitable format for processing over FPGA platform. Face detection system unit is designed using Xilinx System Generator. It is placed between pre-processing and post-processing block.

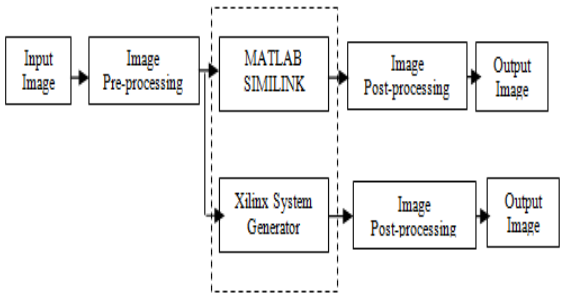

Figure 2: Block diagram for system design

B. System Implementation

In this paper face detection algorithm is implemented over FPGA platform and their comparative analysis is shown. Hardware implementation using XSG is as follow.

Image Pre-processing Block diagram

Image pre-processing is shown in Figure 3. Primary significance of image pre-processing operation is serialization of data with suitable data rate for the hardware implementation [2].

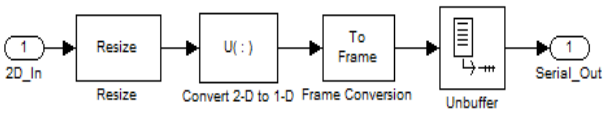

Figure 3: Image Pre-processing block diagram

Image Post-processing Block diagram

Image post-processing is shown in Figure 4.Primary significance of image post-processing is to make

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processed data available and with suitable data rate for displaying in MATLAB environment.

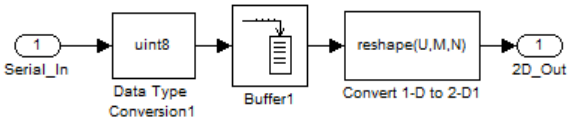

Figure 4: Image Post-processing blockdiagram

c. RGB to YCbCr conversion for Face detection

Image is converted into YCbCr and select particular value of Cb and Cr component such as [90 120] and [140 165] respectively.

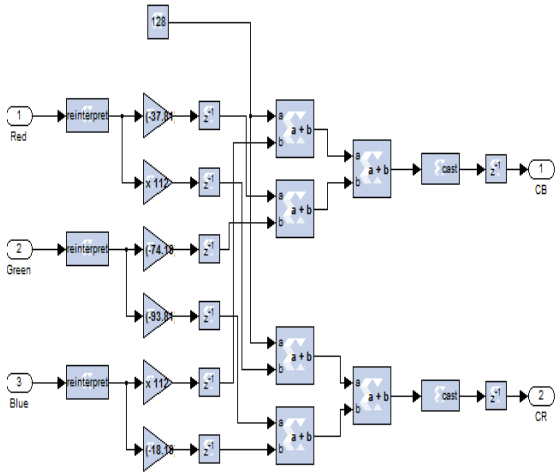

Figure 5: RGB to YCbCr conversion using system generator

d. Erosion and Dilation block for Face detection

After conversion erosion and dilation operation is performed as shown in figure 6 and 7 to remove noise in skin segmentation and finally detect faces from image.

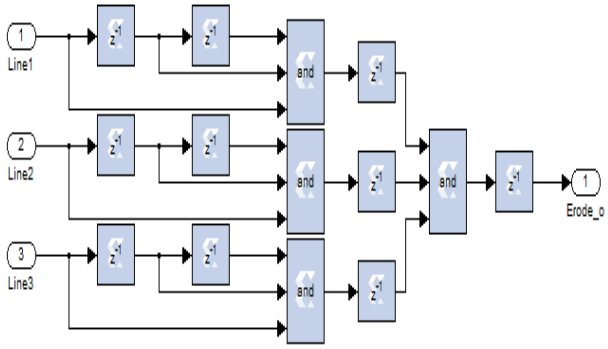

Figure 6: Erosion block using system generator

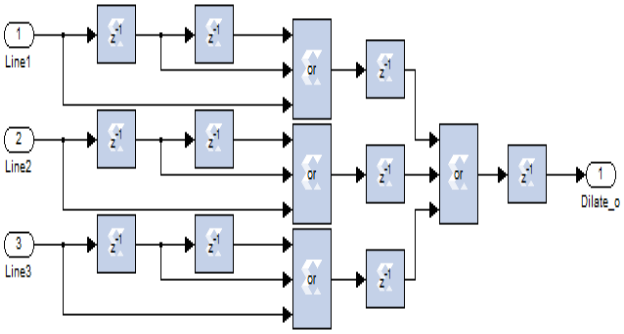

Figure 7: Dilation block using system generator

IV. RESULT

The hardware implementation results are produced using Xilinx Virtex-5 FPGA for face detection system. Figure 8 shows face detection system results using skin color detection for Xilinx system generator and hardware implementation.

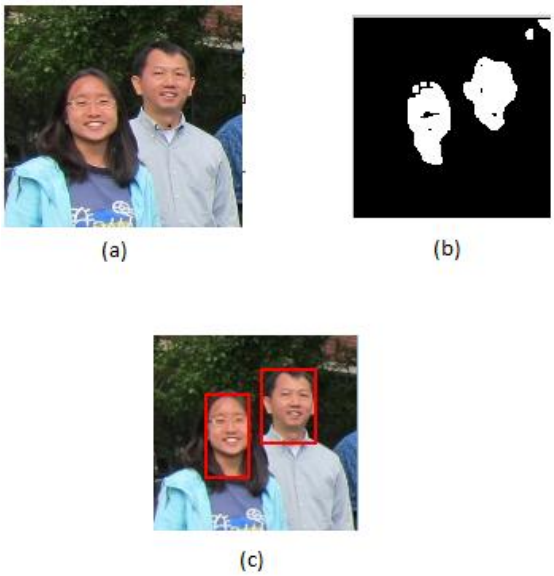

Figure 8: a) Original Image b) Skin Segmentation Image c) FPGA based Face detection

V. CONCLUSION

In this paper skin color detection using YCbCr model algorithm is implemented over Virtex-5 FPGA platform. Skin color is the significant features for image processing and many computer vision applications. The skin detection algorithm presented here is computationally simple and has proved to be very effective. FPGA has high speed multipliers, parallel architecture which makes them superior over their DSP counterparts. The Xilinx System Generator tool of Matlab provides an efficient and simplified approach hardware implementation (FPGA).

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BIOGRAPHIES

Yogesh V. Raut received the B.E. degree in Electronics and Telecommunication Engineering from VPCOE, Baramati, Pune, India in 2012 and is currently pursuing the M.E. degree in VLSI and Embedded systems from MIT College of Engineering, Pune.

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